REMARKS

Applicant acknowledges with appreciation the prospective allowance of claims 7, 8, and 17, subject to overcoming the Examiner's objection to claim 7 upon which claims 8 and 17 are dependent. Claim 7 has been amended, as suggested by the Examiner, so claims 7, 8, and 17 are allowable.

Reconsideration and allowance of claims 1, 5, 14, and 16, "rejected as being unpatentable over Kuriyama et al. (5,550,435) in view of Kojima (5,965,921)," are respectfully requested.

Claims 1, 5, 14, and 16, as amended, recite that the gate electrode is positioned lower than the extraction electrode. The advantage of this feature is that the electron beam path is allowed to converge without a decrease in the field emission amount (see, for example, Figures 6(a) and 6(b) and page 48, lines 17 through 21 and page 61, lines 15 through 16 of Applicant's specification).

Kuriyama et al. describes a field emission cathode apparatus wherein the p-type silicon layer and the n-type silicon layer are positioned above the n^+-type silicon layer (see, for example, Figure 4 of Kuriyama et al.). In Kuriyama et al., the n^+-type silicon layer is described as corresponding to an emitter (extraction) electrode, the n-type silicon layer corresponds to a collector electrode, and the p-type silicon layer corresponds to a base electrode of a bipolar transistor (see column 5, lines 43 through 49). The p-type silicon layer, (i.e., the base electrode) in Kuriyama et al. corresponds to a gate electrode in a field effect transistor (FET). Therefore, it is clear from Kuriyama et al. that the gate electrode would be positioned above the extraction electrode.

Kojima describes a high voltage inverter circuit consisting of MISFET's. The field effect transistors described in Kojima have the gate

electrode positioned above the intermediate gate electrode (see, for example, Figure 17 and column 12, lines 42 through 57 of Kojima). The intermediate gate electrode in Kojima corresponds to the first gate electrode or extraction electrode described in the background art section of Applicant's specification (see page 5, line 2). Kojima, therefore, teaches positioning the gate electrode above the extraction electrode.

Therefore, neither Kuriyama et al. nor Kojima teach or suggest positioning the gate electrode lower than the extraction electrode, so as to achieve the above described advantage. Consequently, claims 1, 5, 14, and 16 are patentable over the combination of Kuriyama et al. and Kojima,

Reconsideration and allowance of claims 2 and 3, "rejected as being unpatentable over Kuriyama et al. and Kojima and further in view of Akamatsu et al. (5,396,096)," are respectfully requested. Claims 2 and 3 are dependent on claim 1 and, therefore, are patentable over the combination of Kuriyama et al. and Kojima for the same reasons advanced above in connection with claim 1. Akamatsu et al. does not make up for the deficiency of the combination of Kuriyama et al. and Kojima. Consequently, claims 2 and 3 are patentable over the combination of Kuriyama et al., Kojima, and Akamatsu et al.

Reconsideration and allowance of claims 4 and 15, "rejected as being unpatentable over Kuriyama et al. (5,550,435) in view of Kojima (5,965,921) and Kawaguchi (JP401061953A)," are respectfully requested.

Claims 4, as amended, and claim 15, dependent on claim 4, recite, similar to claims 1, 5, 14, and 16, that the gate electrode is positioned lower than the extraction electrode. Consequently, Applicant's invention, as defined by claims 4 and 15, is different from and patenable over the combination of Kuriyama

et al. and Kojima for the same reasons advanced above in connection with claims 1, 5, 14, and 16.. Neither Kuriyama et al. nor Kojima teach or suggest positioning the gate electrode lower than the extraction electrode.

Kawaguchi describes a MOS transistor, the object of which is to form a gate without providing an impurity diffusion layer of low concentration and prevent hot carriers being produced in a depletion layer of a drain junction. Referring to the abstract of Kawaguchi, the gate is formed such that a gate width is wider on the drain side of the gate than on the source side.

In Applicant's invention, as recited in claims 4 and 15, a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of the source electrode nearer the source region. Kawaguchi merely discloses that one side of the gate is wider than the other side and does not teach or suggest that the portion of the gate electrode nearer the drain region is wider than a portion of the source electrode nearer the source region.

Furthermore, the unit described in Kawaguchi is not for the purpose of cold electron emission and does not disclose an extraction electrode. As such, Kawaguchi does not teach or suggest positioning the gate electrode lower than the extraction electrode so as to achieve the advantage that electron beam path is allowed to converge without a decrease in the field emission amount.

Consequently, claims 4 and 15 are patentable over the combination of Kuriyama et al., Kojima, and Kawaguchi.

Reconsideration and allowance of claim 6, "rejected as being unpatentable over Kuriyama et al. and Kojima and further in view of Hirano et al. (JP409063467A)," are respectfully requested. Claim 6 is dependent on claim 5 and, therefore, is patentable over Kuriyama et al. and Kojima for the same reasons

advanced above in connection with claim 5. Hirano et al. does not make up for the deficiency of the combination of Kuriyama et al. and Kojima. Consequently, claim 6 is patentable over the combination of Kuriyama et al., Kojima, and Hirano et al.

Reconsideration and allowance of claims 9 and 11 through 13, "rejected as being unpatentable over Kuriyama et al. (5,550435) in view of Hirano et al. (JP409063467A)," are respectfully requested.

In the Office Action dated May 22, 2002, claim 9 and claims 11 through 13, dependent on claim 9, were rejected as being unpatentable over the combination of Kuriyama et al. in view of Hirano et al. In the Amendment dated August 13, 2002, Applicant argued against the rejection of claims 9 and 11 through 13, without amending any of these claims. A final rejection, dated November 4, 2002, was issued with the Kojima reference added to the rejection of claims 9 and 11 through 13 (i.e., a new ground of rejection not necessitated by an amendment made by Applicant). When Applicant pointed out that the final rejection was improper because claims 9 and 11 through 13 were rejected on new grounds not necessitated by an amendment made by Applicant, the Examiner opted to revert to the original rejection of claims 9 and 11 through 13 (i.e., the combination of Kuriyama et al. and Hirano et al.), rather than withdraw the final rejection and leave the rejection of claims 9 and 11 through 13 based on the combination of Kuriyama et al., Kojima, and Hirano et al.

Claims 9 and 11 through 13 are patentable over the combination of Kuriyama et al. and Hirano et al. The Examiner notes correctly in the ***Response to Arguments*** portion of the last Office Action that Applicant has not coneded "that it would be obvious to combine the references (Kuriyama et al. and Hirano et al.)" and that Applicant provided "no specific traverse based on the obviousness

argument presented by the Examiner." In fact, the Examiner did not present, in the May 22, 2002 Office Action, and has not presented, in the last Office Action, any "obviousness argument." All the Examiner has done is identify elements in the two references without providing any support that, when the prior art is taken as a whole, there is a teaching or a suggestion or a motivation for combining the references. In fact, there is no statement in the treatment of claim 9 on page 8 of the May 22, 2002 Office Action nor in the treatment of claim 9 in the paragraph connecting pages 10 and 11 of the last Office Action that it would be obvious to combine the Kuriyama et al. and Hirano et al. references. Thus, the Examiner has not made out a *prima facie* case of obviousness, much less that it would be obvious to combine the Kuriyama et al. and Hirano et al. references, so there has not been any "obviousness argument" to traverse. The Examiner has the burden to make out a *prima facie case* of obviousness --- Applicant does not have the burden to make out a *prima facie* case of a lack of obviousness.

If the Examiner chooses to correct this shortcoming in the rejection of claims 9 and 11 through 13 by providing Applicant, as required, with a complete statement that supports the Section 103 rejection of claims 9 and 11 through 13, the Section 103 rejection of claims 9 and 11 through 13 must be treated as a new grounds of rejection because, until such a statement is provided, Applicant does not know what the Examiner has in mind. A patent applicant is not required to *infer* what an Examiner has in mind.

Reconsideration and allowance of claim 10, "rejected as being unpatentable over Kuriyama et al. and Hirano et al. and further in view of Bergonzoni (4,968,639)," are respectfully requested. Claim 10 is dependent on claim 9 and, therefore, is patentable over Kuriyama et al. and Hirano et al. for the same reasons advanced above in connection with claim 9. Bergonzoni does not

make up for the deficiency of the combination of Kuriyama et al. and Hirano et al. Consequently, claim 10 is patentable over the combination of Kuriyama et al., Hirano et al., and Bergonzoni.

Claims 18 through 22 have been added. Claim 18 is generally similar to claim 9 but has the added limitation that the gate electrode is positioned lower than the extraction electrode. Claims 19 through 22 are similar to claims 10 through 13 but are dependent on claim 18.

Claims 18 through 22 are patentable over the prior art for at least the same reasons advanced above in connection with claims 1 through 6, 10, and 14 through 16. The prior art references neither teach nor suggest positioning the gate electrode lower than the extraction electrode.

Hirano describes a cold electron emitting element and manufacture of such a device. Referring to the abstract and Figure 4 of Hirano et al., the device described is not a field effect transistor, and, as such, does not include a gate region. Therefore, Hirano et al. does not teach positioning the gate electrode lower than the extraction electrode.

In view of the foregoing amendments and remarks, this application is in condition for allowance which action is respectfully requested.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS:

1. (Amended) A field emission type electron source device comprising:

a field emission electron source portion including an extraction electrode provided on a p-type silicon substrate via an insulating film and having an opening portion at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion provided on the p-type silicon substrate, corresponding to the field emission electron source portion,

wherein:

the field emission electron source portion is provided in a drain region of the field effect transistor portion; and a control voltage is applied to a gate electrode of the field effect transistor portion to control a field emission current from the field emission electron source portion, wherein the gate electrode is positioned lower than the extraction electrode;

the drain region includes different impurity elements and includes at least two wells having different impurity concentrations having symmetrical impurity distributions; and

of the at least two wells, one well having a low impurity concentration is provided around a circumference of the other well having a higher impurity concentration.

4. (Amended) A field emission type electron source device comprising:

a field emission electron source portion including an extraction electrode provided on a p-type silicon substrate via an insulating film and having an opening portion at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion provided on the p-type silicon substrate, corresponding to the field emission electron source portion,

wherein:

the field emission electron source portion is provided in a drain region of the field effect transistor portion; and a control voltage is applied to a gate electrode of the field effect transistor portion to control a field emission current from the field emission electron source portion;

the gate electrode of the field effect transistor portion has a shape such that a portion of the gate electrode nearer the drain region has a total width wider than a total width of a portion of the source electrode nearer the source region; [and] a part of the gate electrode is provided in such a manner as to cover an end of the drain region; and the gate electrode is positioned lower than the extraction electrode.

5. (Amended) A field emission type electron source device comprising:

a field emission electron source portion including an extraction electrode provided on a p-type silicon substrate via a first insulating film and having an opening portion at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n-channel field effect transistor portion provided on the p-type silicon substrate, corresponding to the field emission electron source portion,

wherein:

the field emission electron source portion is provided in a drain region of the field effect transistor portion; and a control voltage is applied to a gate electrode of the field effect transistor portion to control a field emission current from the field emission electron source portion, wherein the gate electrode is positioned lower than the extraction electrode;

the drain region including at least two wells having different impurity concentrations, a first of the at least two wells being provided around a circumference of the second of the at least two wells;

a gate insulating film is provided between the gate electrode of the field effect transistor and the p-type silicon substrate; the gate insulating film includes a film thinner than the first insulating film, the first insulating film being provided between the extraction electrode and the p-type silicon substrate; and the gate insulating film is buried with the first insulating film.

7. (Amended) A field emission type electron source device comprising:

a field emission electron source portion including an extraction electrode provided on a p-type silicon substrate via an insulating film and having an opening portion at a position corresponding to a region where a cathode is provided; and a cathode portion provided on the p-type silicon substrate and at a position corresponding to the opening portion of the extraction electrode; and

an n–channel field effect transistor portion provided on the p-type silicon substrate, corresponding to the field emission electrode source portion,

wherein:

the field emission electron source portion is provided in a drain region of the field effect transistor portion; and a control voltage is applied to a

gate electrode of the field effect transistor portion to control a field emission current from the field emission electron source portion;

the field emission type electron source device further comprises a shield electrode made of the same material of that of the gate electrode of the field effect transistor portion, and the shield electrode is provided in such a manner as to cover a channel region of the field effect transistor portion which is not covered with the gate electrode, while the potential of said shield electrode is made to be equal to that of the substrate.

Add new claims 18 through 22.